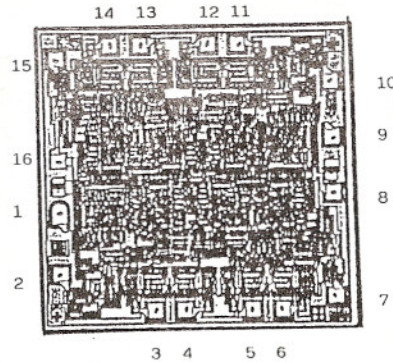




Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



PAD NO	FUNCTIONS
1	CLOCK A
2	ENABLE A
3	Q1A
4	Q2A
5	Q3A
6	Q4A
7	RESET A
8	VSS
9	CLOCK B
10	ENABLE B
11	Q1B
12	Q2B
13	Q3B
14	Q4B
15	RESET B
16	VDD

Topside Metal:
Backside:
Backside Potential:
Mask Ref:
Bond Pads (Mils):

APPROVED BY:
MFG: RCA

DIE SIZE (Mils): 86 X 86
THICKNESS:

DATE: 3/13/00
P/N: CD4518

DG 10.1.2
 Rev A 3-4-99